

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

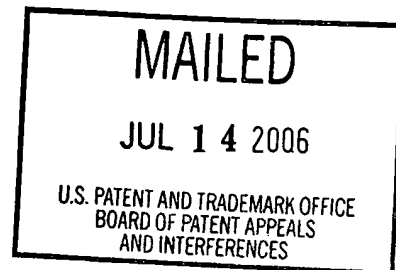
UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DON VAN DYKE, KORBIN VAN DYKE,
and STEPHEN C. PURCELL

Appeal No. 2006-1017
Application No. 09/419,828¹

ON BRIEF



Before RUGGIERO, SAADAT, and HOMERE, Administrative Patent Judges.
SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1, 3-13 and 15-23. Claims 2 and 15 have been canceled.

We reverse.

¹ Application for patent filed October 14, 1999.

BACKGROUND

Appellants' invention is directed generally to an encryption and decryption method under the Data Encryption Standard (DES) such that the DES algorithm is implemented without the need for special purpose modules. Additionally, according to Appellants, using general purpose registers for storing attributes and parameters of the added instruction combines all data flow into a unified data path. An understanding of the invention can be derived from a reading of exemplary independent claim 1, which is reproduced as follows:

1. A computer system capable of performing encryption or decryption under a Data Encryption Standard (DES) algorithm, comprising:

an arithmetic logic unit having a logic circuit for performing expansion permutation, S-box substitution, P-box permutation and associated XOR operations;

wherein said computer system further comprises a register file providing operands to said arithmetic logic unit; and

wherein said register file includes general purpose registers.

The Examiner relies on the following reference:

Jones et al. (Jones)	6,088,800	Jul. 11, 2000
		(filed Feb. 27, 1998)

Appeal No. 2006-1017
Application No. 09/419,828

Claims 1, 3-13 and 15-23 stand rejected under 35 U.S.C.
§ 102(e) as being anticipated by Jones.

We make reference to the answer (mailed September 7, 2005)
for the Examiner's reasoning and to the appeal brief (filed July
11, 2005) for Appellants' arguments thereagainst.

OPINION

Initially, we note that a rejection for anticipation under
section 102 requires that each and every limitation of the
claimed invention be disclosed in a single prior art reference.
In re Paulsen, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed.
Cir. 1994). See also Atlas Powder Co. v. Ireco Inc., 190 F.3d
1342, 1347, 51 USPQ2d 1943, 1946 (Fed. Cir. 1999).

Appellants assert that Jones does not use "general purpose
registers" and instead, avoids using such registers (col. 10,
lines 20-29) by employing specific purpose registers in a
dedicated encryption/decryption processor (brief, page 4).
Appellants further argue that Jones suggests away from the
claimed general purpose processors and the associated general
purpose registers which are used to execute both the DES
algorithm and other instructions (brief, page 5). The Examiner
responds by stating that this portion of Jones does not suggest

Appeal No. 2006-1017
Application No. 09/419,828

that a general-purpose processor cannot be used to accomplish his objective or the simpler arrangement is limited to specific purpose registers (answer, page 10).

We observe that Jones relates to a programmable encryption chip for processing a variety of secret key and public key encryption algorithms (abstract). Jones further teaches that using a dedicated chip reduces complexity by avoiding switch designs and a simpler linear arrangement (col. 10, lines 20-29). Jones' lack of suggestion for excluding general purpose registers notwithstanding and as argued by Appellants (brief, pages 3 & 5), by using special purpose registers, the reference provides for a dedicated encryption process which would be different from the claimed "general purpose registers."

Additionally, referring to Figure 3 and its corresponding description (col. 7, lines 15-38), Appellants point out that using ALU 56 operating on 32-bit words from the register file 58 of Jones does not describe or suggest the claimed register file including general purpose registers (brief, page 6). In response to Appellants' arguments, the Examiner asserts that Jones discloses that the registers can be used as an operand to any

instruction which allows them to be a general purpose register (answer, page 11). The Examiner further asserts that, since "the same architecture is being used, the registers are not used for only a specific purpose but are addressable depending on the type of instruction ..." (id.).

As correctly identified by Appellants, Jones specifically avoids complexity by processing the algorithm using dedicated registers (col. 10, lines 25-29). Although the Examiner asserts that the registers of Jones function in the same manner as Appellants' registers when they perform an encryption process (answer, page 12), the Examiner does not point to, nor do we find any, teaching in Jones indicating that the registers are general purpose registers. What a reference teaches is a question of fact. In re Baird, 16 F.3d 380, 382, 29 USPQ2d 1550, 1552 (Fed. Cir. 1994) (citing In re Beattie, 974 F.2d 1309, 1311, 24 USPQ2d 1040, 1041 (Fed. Cir. 1992)). In fact, while all types of registers store information, the portions in Jones identified by Appellants actually provide more evidence demonstrating that the registers are dedicated and assigned to the processor for the encryption.

Appeal No. 2006-1017
Application No. 09/419,828

In view of the discussion above and the weight of evidence presented by Appellants and the Examiner, we find that the use of general purpose registers, as recited in independent claims 1, 13 and 22, are absent in Jones. Accordingly, since the Examiner has failed to meet the burden of providing a prima facie case of anticipation, the 35 U.S.C. § 102 rejection of claims 1, 3-13 and 15-23 over Jones cannot be sustained.

Application No. 09/419,828

CONCLUSION

1, 3-13 and 15-23 under 35 U.S.C. § 102 is reversed.

REVERSED

JOSEPH F. RUGGIERO

JOSEPH F. RUGGIERO
Administrative Patent Judge

Manfred W. Gaudart

MAHSHID D. SAADAT
Administrative Patent Judge

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APPEALS
AND
INTERFERENCES

Jean R. Homere

JEAN R. HOMERE
Administrative Patent Judge

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Appeal No. 2006-1017
Application No. 09/419,828

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